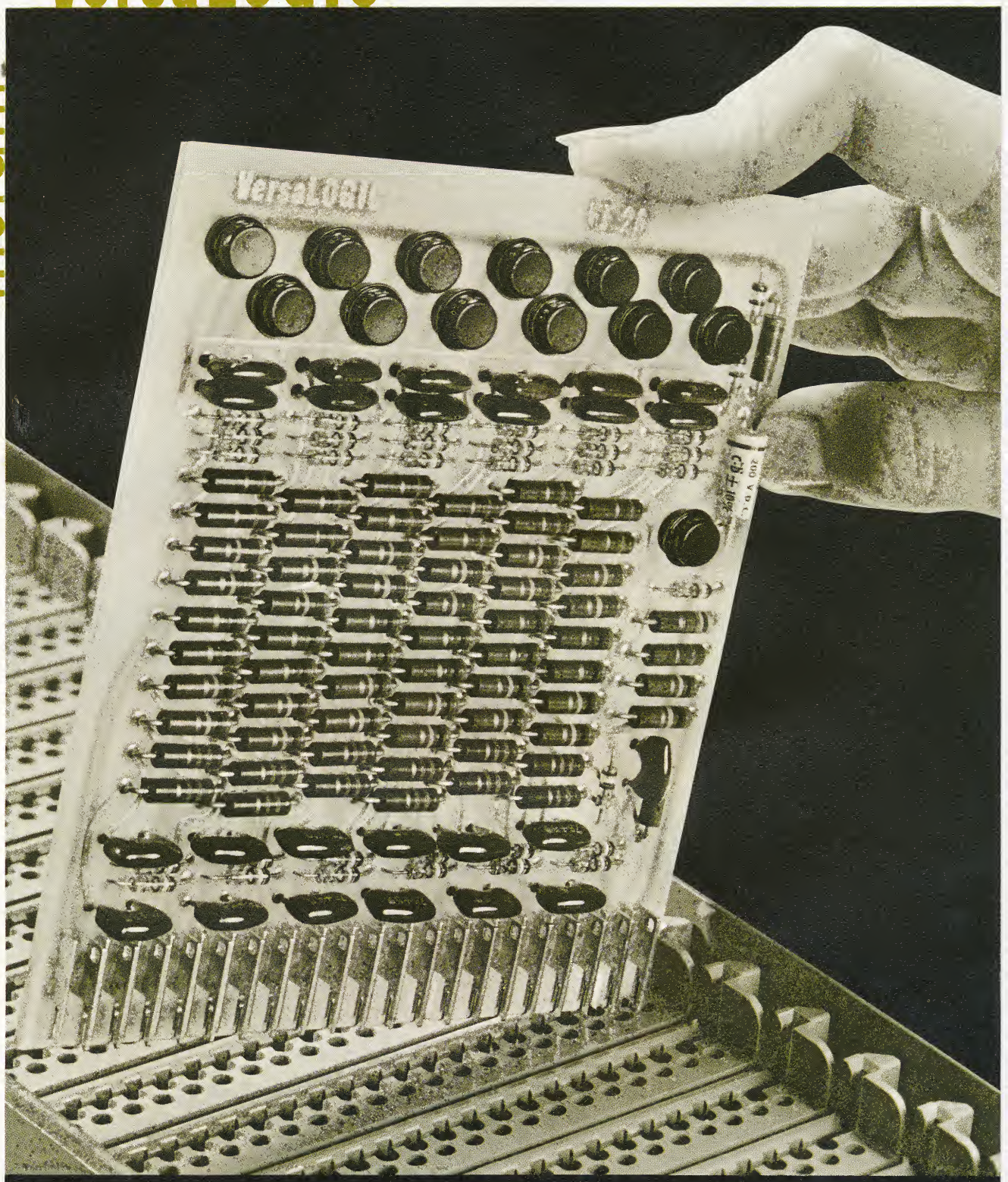
digital system modules - 200kc - 2mc - 8mc

VersaLOGIC

instant

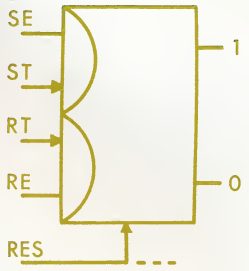


the VersaLOGIC concept for
the engineer in a hurry...

DECISION CONTROL, INC.

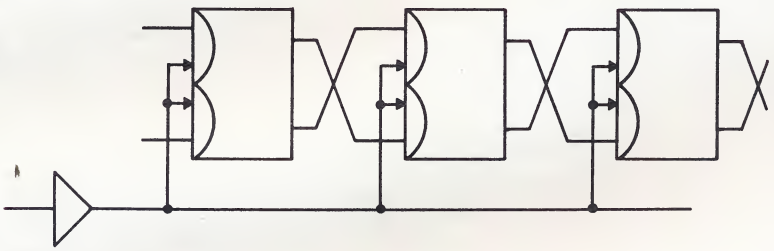
The VersaLOGIC concept is the *system* concept . . . digital modules developed by systems experts for systems applications. That's why each step of the total system job, initial logic to working hardware, is done better *and* more efficiently with VersaLOGIC. To cut design time, three basic circuits with simple logic rules are used . . .

System Flip Flop



The VersaLOGIC System Flip Flop is a two-transistor circuit controlled by single SET and RESET gates. Each gate has an ENABLE (dc) and a TRIGGER (ac) input. A gate is activated whenever a ground level is established on an ENABLE input and a positive-going pulse is applied to the corresponding TRIGGER input. The ENABLE inputs are used to set the logic conditions that determine the next state the flip flop is to assume. The TRIGGER inputs then determine when the flip flop will respond to these conditions.

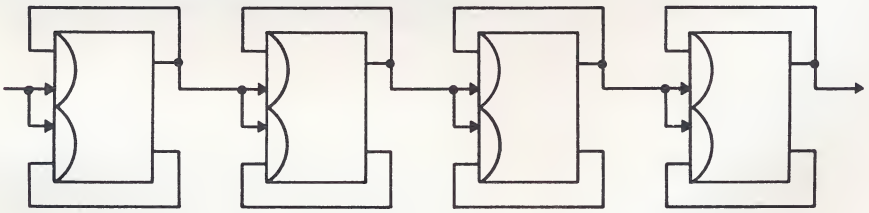
In the VersaLOGIC convention 0 volts represents logic '0' and -10 volts represents logic '1'. According to this convention, the *complement* of the enabling logic function is used at the corresponding ENABLE input. For example, a simple shift register is wired with each flip flop '0' output



shift register

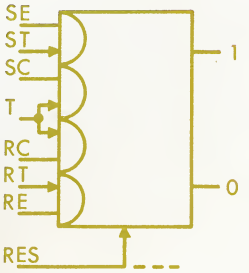
forming the SET ENABLE, and each '1' output the RESET ENABLE, for the next stage in the register.

If the '1' and '0' outputs of a flip flop are fed back to the SET ENABLE and RESET ENABLE inputs respectively, the flip flop will be steered to toggle whenever the TRIGGER inputs are pulsed. An asynchronous binary counter is therefore implemented in this way:



binary counter

Universal Flip Flop

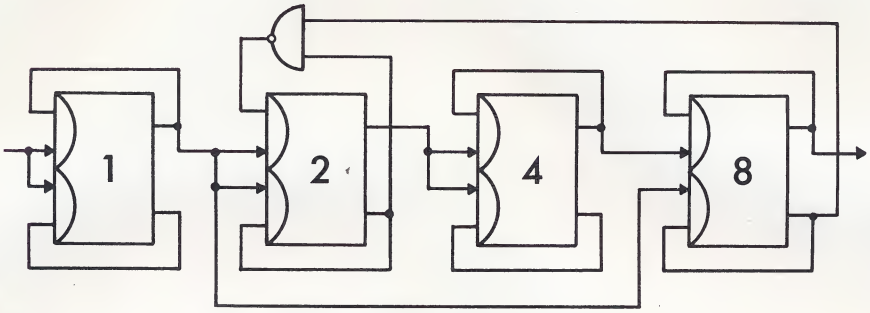


Shift right - shift left registers, parallel-to-serial conversion registers and similar problems are implemented by the VersaLOGIC Universal Flip Flop. This flip flop is identical to the one above except that a second pair of ENABLE gates with common TRIGGER inputs is added.

All VersaLOGIC flip flops have a common reset driver shared by all flip flops on a card. It provides a high speed reset or preset for counters and registers.

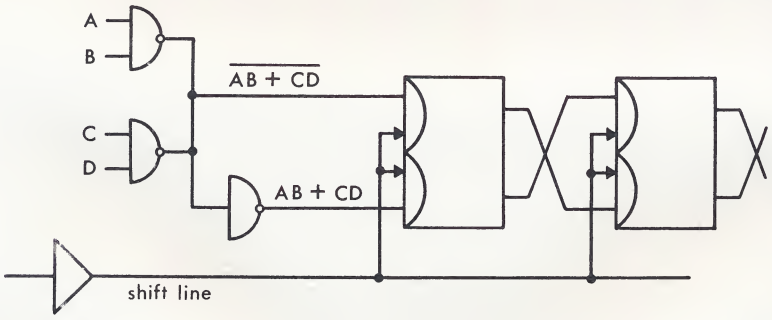
System NAND Gate / Expandable NAND Gate

Logic functions for controlling the ENABLE points are built from VersaLOGIC NAND Gates. These circuits have a 3-diode AND gate input with inverting amplifier output. The Expandable NAND Gate can be increased to 12 inputs by connecting extra diode groups to the common point. The System NAND Gate, which does over 90% of the gating in typical systems, is non-expandable for maximum packing density. A binary-coded-decimal counter is built from VersaLOGIC System components as shown:



bcd counter 8421 code

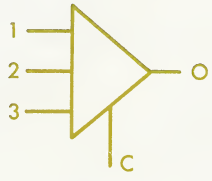
All VersaLOGIC NAND Gates are unloaded to allow either individual operation or connection of gates in parallel. Twelve gates may be connected to a common load resistor. When two or more NAND gates share a load resistor the complement of the logical AND/OR function results. The output of a NAND gate or several paralleled gates therefore represents the desired signal for an ENABLE input when a true condition exists on the gate inputs. For example, to enter the function F = AB + CD into a shift register the output of the gating structure is taken directly to the SET ENABLE input of the flip flop. The RESET ENABLE input is formed by using a second gate to invert the function.



gated shift register

Power Amplifier

System clocks and functions which must be taken to many inputs require more capacitive or current driving capability than is practical to provide from flip flops or gates. The VersaLOGIC Power Amplifier provides this drive. The power amplifier has a 3-input AND gate, expandable to 12 inputs, and is non-inverting. These features allow great versatility in system clock distribution and adapt the power amplifier to many important decoding and logic operations as well.



system engineered

VersaLOGIC *builds*

. . . reliable hardware

. . . quickly

. . . economically

VersaLOGIC performance . . . and cost . . . is readily matched to system needs. Full signal and packaging compatibility among the three series of VersaLOGIC makes mixed system designs highly practical.

SPEEDS

	Maximum Clocked Frequency	Propagation Time (Typical)
Series 10	*200kc*	*500ns*
Series 20	*2mc*	*50ns*
Series 30	*8mc*	*15ns*

To eliminate guesswork, loading rules are few and clearly stated. These are given in terms of a standard load and circuit drive capability.

LOADING

Gate Input	=	**1**	*load*
Enable Input	=	**2**	*loads*
Trigger Input	=	**4**	*loads*
1 *series 10 load*	=	**2**	*series 20 loads*
1 *series 30 load*	=	**2½**	*series 20 loads*

In all cases, circuit drive is specified as worst case with a generous allowance for stray wiring capacitance.

DRIVE

	Series 10/20	Series 30
Flip Flop	**12** *loads*	**8** *loads*
NAND Gate	**6**	**4**
Power Amplifier	**48**	**24**

High density packaging of identical circuits results in low system costs.

PACKAGING

	Series 10/20	Series 30
System Flip Flop	**6**/*card*	**4**/*card*
Universal Flip Flop	**4**	**2**
System NAND Gate	**8**	**6**
Expandable NAND Gate	**4**	**4**
Power Amplifier	**6**	**4**

Systematic, standardized pin layout on VersaLOGIC connectors cuts errors and hours from the production of wiring diagrams.

For low power dissipation and high system reliability, VersaLOGIC uses only two supply voltages.

POWER

Voltages:	*-12v and +6v, both ±10%*		
Dissipation:	**Series 10**	**Series 20**	**Series 30**
Flip Flop	*165mw*	*200mw*	*375mw*
NAND Gate	*96*	*88*	*184*
Power Amplifier	*200*	*200*	*400*

Solid logic levels are assured since all VersaLOGIC loads are returned to -12 volts and are driven by a saturated transistor to ground.

GENERAL

Logic 0	*0v nominal, 1v min. noise rejection*
Logic 1	*-10v nominal, 2v min. noise rejection*
Temperature	*-10°C to +55°C*
Card	*Glass epoxy, 4.3"x 5.2"*
Wiring	*Taper pin, solder tab, or wire wrap*

VersaLOGIC systems cannot be harmed by miswiring . . . are immune to scope probe accidents. To speed checkout and maintenance, all circuits are protected against damage from shorting or grounding the exposed connector pins.

THE FIVE BASIC VersaLOGIC modules are backed by a full line of system accessories: standard circuit cards — Crystal Clock, DMV, etc. — as well as special designs to customer requirements, memories, power supplies, and mounting hardware. VersaLOGIC Card Frames mount 25 cards in 5¼" of panel space, may be used for either rack or drawer assemblies . . . power and ground busses are prewired, module positions and pin numbers are clearly marked.

dci **DECISION CONTROL, INC.**

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